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(71) Applicant: Agilent Technologies, Inc. (a Delaware corporation)
Palo Alto, CA 94303 (US)

(72) Inventors:
• Roth, Bernhard
71032 Böblingen (DE)
• Ossoinig, Henriette
70197 Stuttgart (DE)

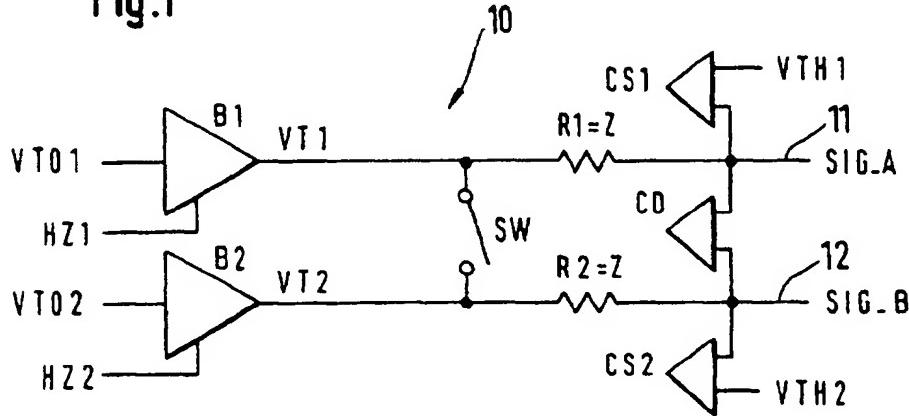
(74) Representative: Barth, Daniel et al
c/o Agilent Technologies Deutschland GmbH,
Patentabteilung, Herrenbergerstrasse 130
71034 Böblingen (DE)

(54) Automatic test equipment for testing a device under test

(57) An electronic circuit (10) for an automatic test equipment for testing a device under test is described. Two lines (11, 12) are present for connecting the circuit with a device under test. Two comparators (CS1, CS2) are provided, one input of each of the comparators (CS1, CS2) being connected to different ones of the two lines (11, 12). A further comparator (CD) is provided, the

two inputs of the further comparator (CD) being connected to different ones of the two lines (11, 12). Each of the two lines (11, 12) is terminated. Switching elements are provided which are connected between the two lines (11, 12). The switching elements enable the circuit (10) to be used in different modes, in particular with a single-ended termination and with a differential termination.

Fig.1



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Description**Background of the Invention**

[0001] The invention relates to an electronic circuit for automatic test equipment for testing a device under test.

[0002] Automatic test equipment is generally known and widely used for testing a variety of different electronic devices. The test equipment comprises a so-called pin-electronic circuit for generating input signals to the device under test. This circuit also has to represent a correct termination for the device under test and, finally, must be capable to analyze the response signals from the device under test.

[0003] As a first possibility, the device under test may have one physical signal line for any one of the logical signals. This case is called single-ended. In this case, the pin-electronic circuit may be terminated e.g. via a resistor to a programmable voltage.

[0004] As a second possibility, the device under test has differential output signals, i.e. two lines per signal. In this case, the pin-electronic circuit may be terminated with one resistor at each line of the differential signal wherein the two resistors of the two lines are programmed to the same voltage. This is called a differential signal operation with single-ended termination. As well, the pin-electronic circuit may be terminated with one resistor between both lines of the differential signal. This is called a differential signal operation with differential termination.

[0005] Due to these different possibilities, different pin-electronic circuits and therefore different automatic test equipments are necessary for testing the different devices under test. This results in increased efforts and costs.

Object and Advantages of the Invention

[0006] It is therefore an object of the invention to provide an improved automatic test equipment, which requires less efforts and costs.

[0007] This object is solved by an electronic circuit for an automatic test equipment according to claim 1.

[0008] The invention provides the advantage that one and the same circuit may be used for an independent single-ended termination of any of the lines of the device under test, for a differential signal operation with single-ended termination and for a differential signal operation with differential termination. As a result, one and the same circuit may be used for different devices under test. Or in other words: It is not necessary anymore to provide different circuits for these different devices under test. The effort and the costs in connection with the automatic test equipment are therefore reduced.

[0009] In an embodiment of the invention according to claim 2, a diode bridge is used to switch between the different modes of the electronic circuit according to the invention. This diode bridge has the advantage that the

automatic test equipment may be implemented for high-frequency applications because it can be made on one semiconductor chip, which minimizes physical distances.

5 [0010] Further embodiments of the invention are provided in the other dependant claims.

Detailed Description of an Embodiment of the Invention

10 [0011] Figure 1 shows a first embodiment of an electronic circuit for an automatic test equipment according to the invention, figure 2 shows a second embodiment of an electronic circuit according to the invention, and figure 3 shows a third embodiment of an electronic circuit according to the invention.

[0012] In figure 1, a first embodiment of a pin-electronic circuit 10 for an automatic test equipment according to the invention is shown.

[0013] A signal SIG_A from a device under test is received by the circuit 10 on a line 11 and a signal SIG_B from the same device under test is received by the circuit 10 on a line 12. One input of a comparator CS1 is connected to the line 11 and one input of a comparator CS2 is connected to the line 12. The respective other inputs of the comparators CS1, CS2 receive a voltage VTH1, VTH2. The two inputs of another comparator CD are connected to the two lines 11, 12.

[0014] Each of the two lines 11, 12 are also connected to a resistor R1, R2 which both have the impedance Z of each of the transmission lines from the device under test to the circuit 10. The other sides of two resistors R1, R2 are then connected together via a switch SW.

[0015] Two buffers B1, B2 generate voltages VT1, VT2 at their outputs. The value of these voltages VT1,

35 VT2 may be varied by voltages VT01, VT02 at the inputs of the buffers B1, B2. The outputs of the buffers B1, B2 are connected to the resistors R1, R2 at both sides of the switch SW. The voltages VT1, VT2 of the buffers B1, B2, therefore, constitute respective terminations for the two lines 11, 12.

[0016] If the signals SIG_A, SIG_B on the lines 11, 12 do not require any termination, then the buffers B1, B2 may be switched into a high-impedance state with the signals HZ1, HZ2.

45 [0017] If the switch SW is open as shown in figure 1, the circuit 10 of figure 1 provides a single-ended termination for the lines 11, 12. The line 11 and the line 12 are independent of each other. E.g. the line 11 may be terminated with the voltage VT1 by the buffer B1. Then,

50 the signal SIG_A of the line 11 may be compared with the voltage VTH1 by the comparator CS1. At the same time, the buffer B2 may be switched into a high-impedance state and the signal SIG_B of the line 12 may be compared with the voltage VTH2 by the comparator CS2. In this case, the comparator CD is inactive.

[0018] If the switch SW is open as shown in figure 1 and if the input voltages VT01, VT02 of the two buffers B1, B2 are selected such that the output voltages VT1,

VT2 of the buffers B1, B2 are identical, then the circuit 10 of figure 1 provides a differential signal operation with a single-ended termination. In one embodiment, the two comparators CS1, CS2 are inactive and the two signals SIG_A, SIG_B are compared by the comparator CD. In another embodiment, the comparison may be performed by the two comparators CS1, CS2 with the comparator CD being inactive.

[0019] If the switch SW is closed and if the two buffers B1, B2 are put into their high-impedance state, the circuit 10 of figure 1 provides a differential signal operation with a differential termination. In this case, the two comparators CS1, CS2 are inactive and the two signals SIG_A, SIG_B are compared by the comparator CD.

[0020] Figure 2 shows a second embodiment of a pin-electronic circuit 20 of an automatic test equipment according to the invention. The circuit 20 of figure 2 is similar to the circuit 10 of figure 1. Therefore, corresponding features are depicted with the same reference characters.

[0021] In figure 2, the switch SW of figure 1 is replaced by a diode bridge 21 and two switched current sources 22, 23. The diode bridge 21 comprises four diodes D1, D2, D3, D4. A serial connection of a current source 11 and a switch SW1 is connected to the anodes of the diodes D1, D2. The cathodes of the diodes D3, D4 are connected to a serial connection of a switch SW2 and a current source 12. The cathode of the diode D1 is connected to the anode of the diode D3 and both are connected to a connection point of two resistors R10, R11. The other side of the resistor R10 is connected to the output of the buffer B1 and the other side of the resistor R11 is connected to the line 11. The cathode of the diode D2 is connected to the anode of the diode D4 and both are connected to a connection point of two resistors R20, R21. The other side of the resistor R20 is connected to the output of the buffer B2 and the other side of the resistor R21 is connected to the line 12. The two switches SW1, SW2 may be switched with the help of a common signal DT.

[0022] The diode bridge 21 is used in its non-resistive region so that it acts as a current source or a current sink.

[0023] If the two buffers B1, B2 are in their low-impedance state and if the two switches SW1, SW2 are open as shown in figure 2 due to a low signal DT, the circuit 20 of figure 2 provides a single-ended termination for the two lines 11, 12. The comparators CS1, CS2 are active whereas the diode bridge 21 and the comparator CD are inactive. The termination of each of the two lines 11, 12 may be programmed differently by the input voltages VT01, VT02 of the buffers B1, B2. The resistors R10, R11 and the resistors R20, R21 may be selected such that they result in the impedance Z of each of the transmission lines from the device under test to the two lines 11, 12.

[0024] If the input voltages VT01, VT02 of the two buffers B1, B2 are selected such that the output voltages

VT1, VT2 of the buffers B1, B2 are identical, and if the two switches SW1, SW2 are open, then the circuit 20 of figure 2 provides a differential signal operation with single-ended termination.

5 [0025] If the two buffers B1, B2 are in their high-impedance state and if the two switches SW1, SW2 are closed due to a high signal DT, the circuit 20 of figure 2 provides a differential signal operation with differential termination of the lines 11, 12. The diode bridge 21 and the comparator CD are active whereas the comparators CS1, CS2 are inactive.

[0026] In a further embodiment, the diode bridge 21 may also be used in its resistive region so that it acts as a so-called active or programmable load for one of the two lines 11, 12. In this case, the two switches SW1, SW2 are closed and e.g. the buffer B1 is set into its high-impedance state and the buffer B2 is set into its low-impedance state at a first voltage. If e.g. the line 11 carries a second voltage, then the voltage difference between the first and the second voltage is present at the diode bridge 21. As a result, the diode bridge 21 represents a load, which is programmable in particular with the first voltage and therefore the output voltage of the buffer B2.

20 [0027] Figure 3 shows a third embodiment of a pin-electronic circuit 30 of an automatic test equipment according to the invention. The circuit 30 of figure 3 is similar to the circuit 20 of figure 2. Therefore, corresponding features are depicted with the same reference characters.

[0028] In figure 3, the two buffers B1, B2 of figure 1 are replaced by two drivers DR1, DR2. Each of these drivers DR1, DR2 has an input, which may be programmed with a voltage DATA1, DATA2.

25 [0029] In a first mode, the voltages DATA1, DATA2 may be programmed identical to the voltages VT01, VT02 as described in connection with the circuit 20 of figure 2. In this mode, the drivers DR1, DR2 of the circuit 30 of figure 3 are used to establish a termination for the two lines 11, 12. This mode, therefore, is used for receiving the signals SIG_A, SIG_B on the lines 11, 12 from the device under test.

[0030] However, the two drivers DR1, DR2 may also be used to send signals via the two lines 11, 12 to the device under test, in particular a logical low level signal or a logical high level signal. In this mode, the inputs DATA1, DATA2 of the drivers DR1, DR2 are programmed as desired by a specific test program included in the automatic test equipment.

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Claims

- 55 1. Electronic circuit (10, 20, 30) for an automatic test equipment for testing a device under test, comprising: two lines (11, 12) for connecting the circuit with the device under test, two comparators (CS1, CS2), one input of each of the comparators (CS1, CS2)

being connected to different ones of the two lines (11, 12), a further comparator (CD), the two inputs of the further comparator (CD) being connected to different ones of the two lines (11, 12), elements for terminating each of the two lines (11, 12), and switching elements being connected between the two lines (11, 12).

2. Circuit (10, 20, 30) according to claim 1 wherein the switching elements being connected between the two lines (11, 12) such that the circuit (10, 20, 30) may be used for a single-ended termination or for a differential termination.
3. Circuit (20, 30) according to claim 1, the switching elements comprising a diode bridge (21) being serially connected to two switched current sources (22, 23).
4. Circuit (20, 30) according to claim 3, the switched current sources (22, 23) each comprising a serial connection of a current source (I1, I2) and a switch (SW1, SW2).
5. Circuit (20, 30) according to claim 3 wherein the diode bridge (21) may be used as a so-called active or programmable load.
6. Circuit (10, 20) according to claim 1, the elements for terminating comprising a buffer (B1, B2) and at least one resistor (R1, R2, R10, R11, R20, R21) for each of the lines (11, 12), wherein the output of the buffer (B1) is connected to the respective line (11) via the respective resistor/s (R1, R10, R11).
7. Circuit (30) according to claim 1, the elements for terminating comprising a driver (DR1, DR2) and at least one resistor (R1, R2, R10, R11, R20, R21) for each of the lines (11, 12), wherein the output of the driver (DR1) is connected to the respective line (11) via the respective resistor/s (R1, R10, R11).
8. Circuit (30) according to claim 7, the switching elements comprising a diode bridge (21) being serially connected to two switched current sources (22, 23).
9. Circuit (30) according to claim 8, the diode bridge (21) being connected between the two lines (11, 12).
10. Circuit (30) according to claim 9, the elements for terminating comprising two resistors (R10, R11, R20, R21) for each of the lines (11, 12) and the diode bridge (21) being connected to the connection point of the two resistors (10, 11, 20, 21) of each of the lines (11, 12).
11. Circuit (30) according to claim 8, the switched cur-

rent sources (22, 23) each comprising a serial connection of a current source (I1, I2) and a switch (SW1, SW2).

Fig.1

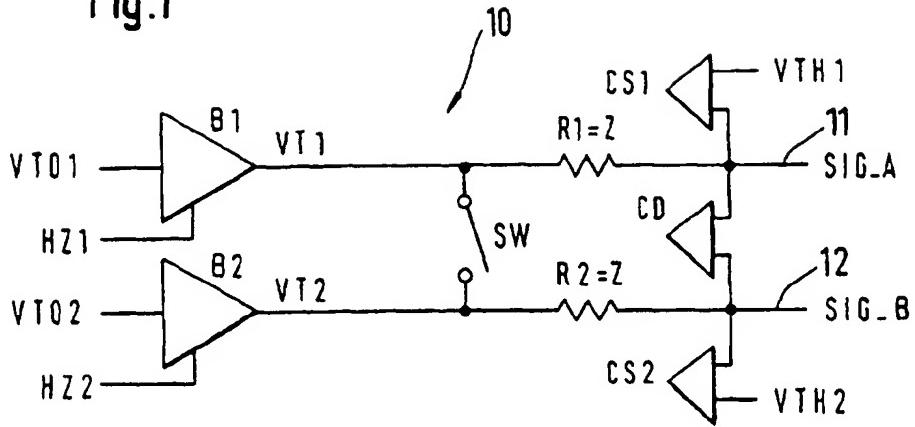


Fig.2

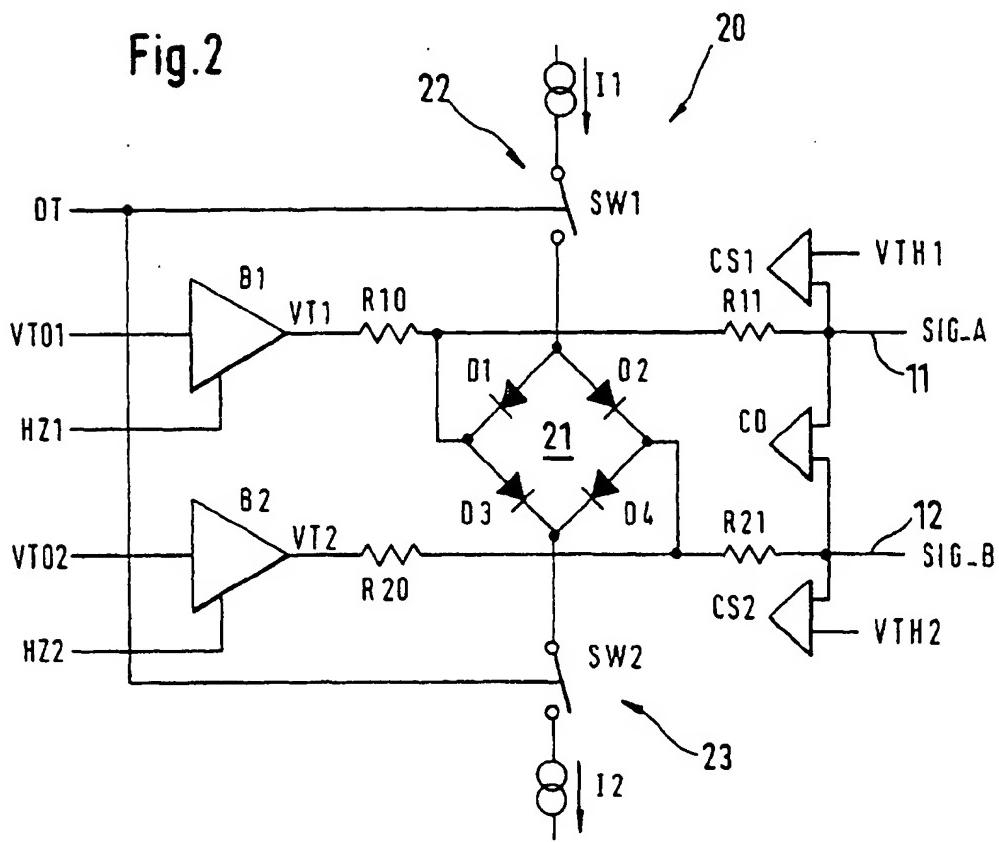
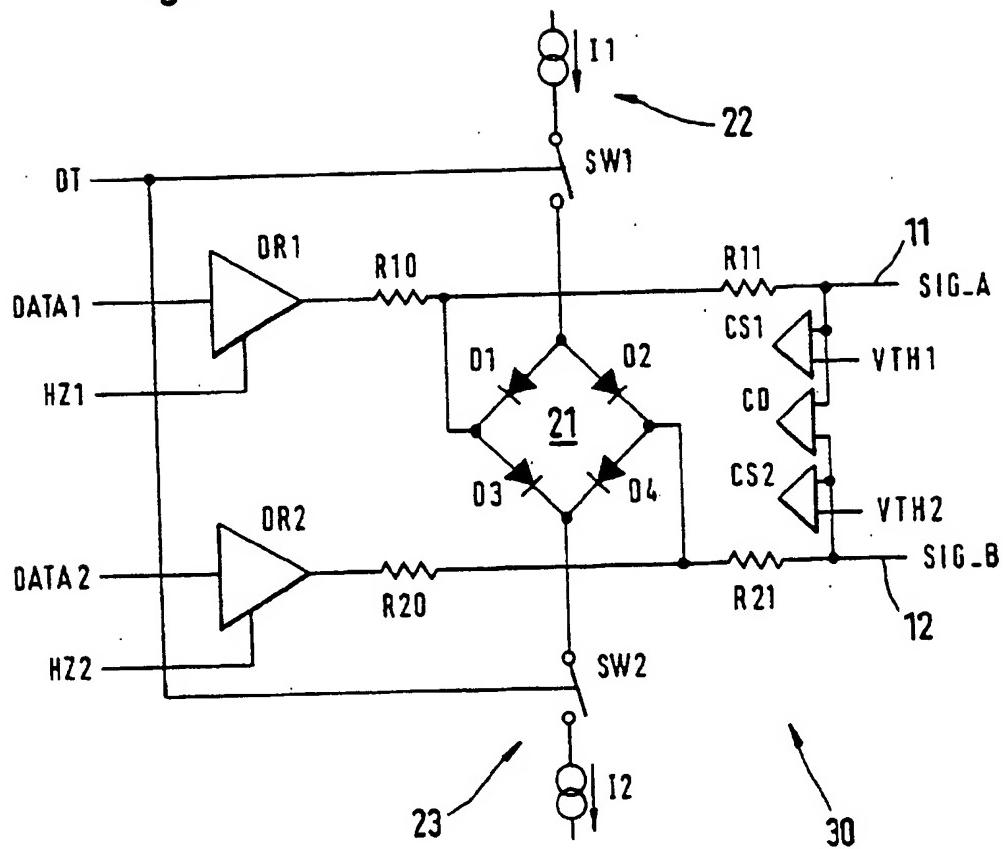


Fig.3





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EUROPEAN SEARCH REPORT

Application Number
EP 01 10 5970

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 101 153 A (MORONG III WILLIAM H) 31 March 1992 (1992-03-31) * abstract; figures 1,3,7 * * column 18, line 65 - line 68 * ---	1-11	G01R31/28
A	US 6 016 566 A (YOSHIDA KENJI) 18 January 2000 (2000-01-18) * abstract; figure 1 *	1,7	
A	WO 99 52203 A (CREDENCE SYSTEMS CORP) 14 October 1999 (1999-10-14) * abstract; figures 7,9 *	1	
A	US 5 521 493 A (PERSONS THOMAS W) 28 May 1996 (1996-05-28) * abstract; figures 2,4 *	3-8	
A	US 5 010 297 A (BABCOCK DOUGLAS W) 23 April 1991 (1991-04-23) * abstract; figure 1 *	3-8,11	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			G01R
The present search report has been drawn up for all claims			
Place of search BERLIN	Date of completion of the search 24 August 2001	Examiner Fritz, S	
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ON EUROPEAN PATENT APPLICATION NO.**

EP 01 10 5970

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Patent document cited in search report		Publication date	Patent family member(s)			Publication date
US 5101153	A	31-03-1992	NONE			
US 6016566	A	18-01-2000	JP	9197018	A	31-07-1997
			DE	19780110	T	12-02-1998
			GB	2314712	A,B	07-01-1998
			WO	9727493	A	31-07-1997
WO 9952203	A	14-10-1999	US	5942922	A	24-08-1999
			EP	1070385	A	24-01-2001
			US	6057716	A	02-05-2000
US 5521493	A	28-05-1996	NONE			
US 5010297	A	23-04-1991	NONE			

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